AND8282/D

Implementing Cost Effective and Robust Power Factor Correction with the NCP1606

Prepared by: Jon Kraft
ON Semiconductor

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APPLICATION NOTE

Introduction

The NCP1606 is a voltage mode power factor correction (PFC) controller designed to drive cost−effective pre−converters to meet input line harmonic regulations. The device operates in Critical Conduction Mode (CRM) for optimal performance in applications up to about 300 W. Its voltage mode scheme enables it to obtain unity power factor without the need for a line sensing network. The output voltage is accurately controlled with a built in high precision error amplifier. The controller also implements a comprehensive array of safety features for robust designs.

This application note describes the design and implementation of a 400 V, 100 W, CRM Boost PFC pre−converter using the NCP1606. The converter exhibits high power factor, low standby power dissipation, good active mode efficiency, and a variety of protection features.

The Need for PFC

Most electronic ballasts and switching power supplies use a diode bridge rectifier and a bulk storage capacitor to produce a dc voltage from the utility ac line. This produces a non−sinusoidal current draw and places a significant demand on the power delivery infrastructure. Increasingly, government regulations and utility requirements often necessitate control over line current harmonic content.

Active PFC circuits have become the most popular way to meet these harmonic content requirements. They consist of inserting a PFC pre−regulator between the rectifier bridge and the bulk capacitor (Figure 1). The boost (or step−up) converter is the most popular topology for active power factor correction. With the proper control, it can be made to produce a constant output voltage while drawing a sinusoidal current from the line.

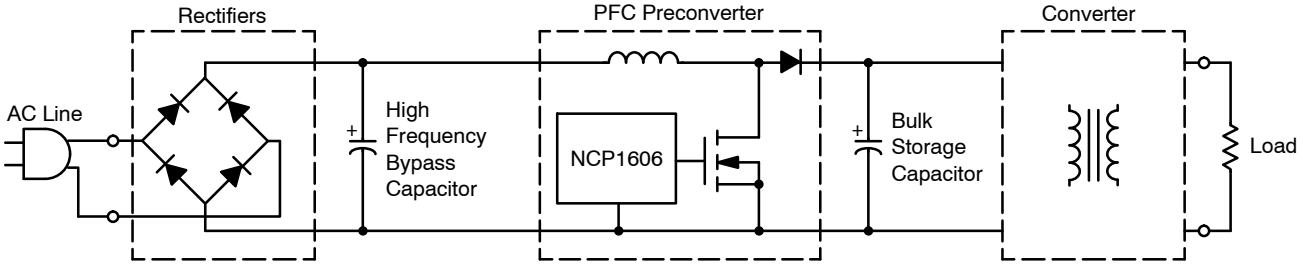

Figure 1. Active PFC Stage with the NCP1606

Basic Operation of a CRM Boost Converter

For medium power (<300 W) applications, critical conduction mode (CRM) is the preferred control method. Critical conduction mode occurs at the boundary between discontinuous conduction mode (DCM) and continuous conduction mode (CCM). In CRM, the next driver on time is initiated when the boost inductor current reaches zero. Hence, CRM combines the lower peak currents of CCM operation with the zero current switching of DCM operation. But this control method means that the frequency inherently varies with the line input voltage and the output load. The operation and waveforms in a PFC boost converter are illustrated in Figure 2. For detailed information on the operation of a CRM Boost Converter for PFC applications, please refer to AND8123 at www.onsemi.com.

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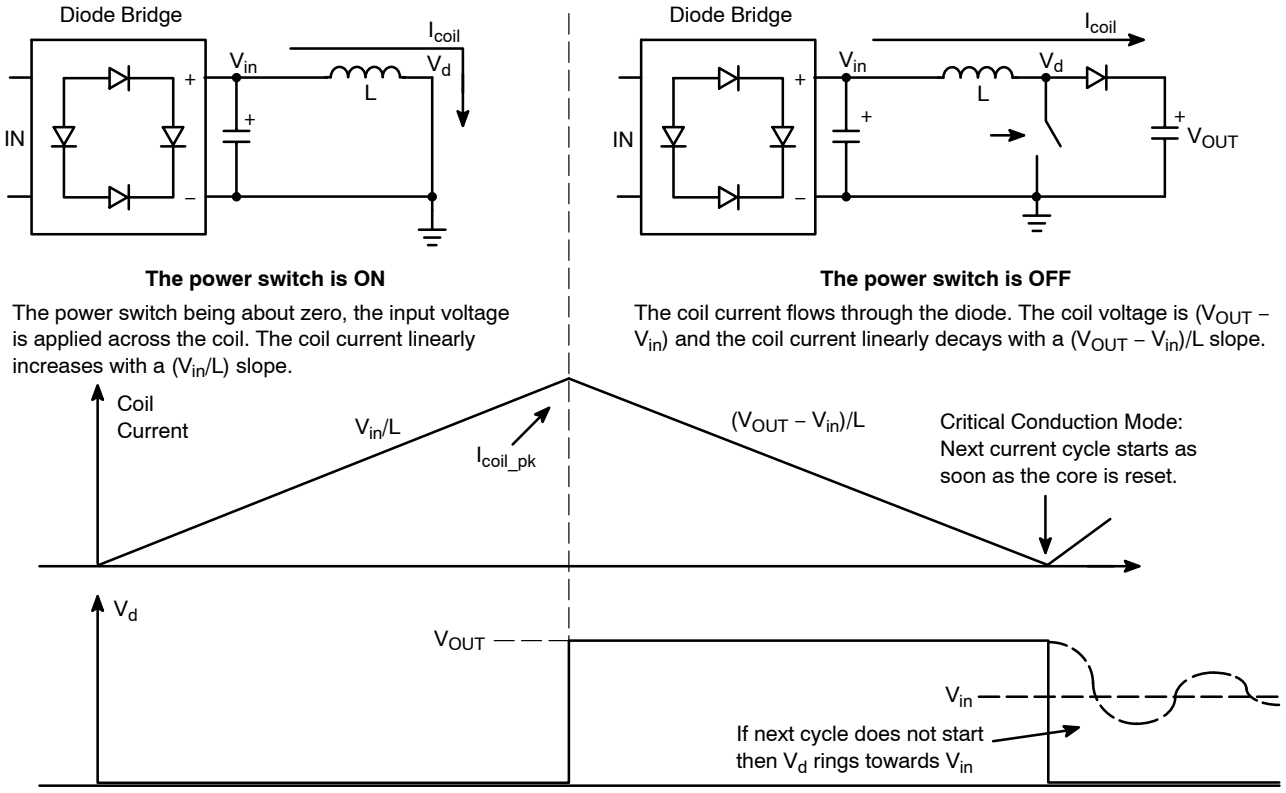

Figure 2. Schematic and Waveforms of an Ideal CRM Boost Converter

Features of the NCP1606

The NCP1606 offers an ideal controller for these medium power CRM boost PFC applications. A simple CRM Boost pre−converter featuring the NCP1606 is shown in Figure 3.

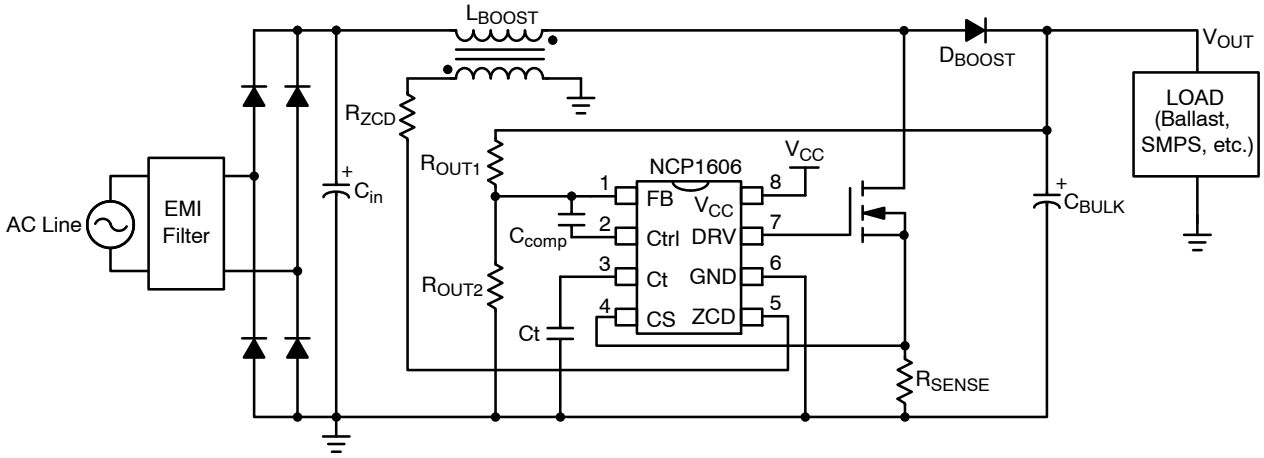

Figure 3. CRM Boost PFC Stage Featuring the NCP1606

Pin 1 (FB) senses the boost output voltage through the resistor divider formed by R_{OUT1} and R_{OUT2}. This pin is the input to an error amplifier, whose output is pin 2 (Control). A combination of resistors and capacitors between these pins form a compensation network that limits the bandwidth of the converter. For good power factor, this bandwidth is generally below 20 Hz. A capacitor connected to pin 3 (Ct) sets the on time for a given Control voltage. The combination of these three pins provides excellent power factor and an accurately controlled output voltage.

CS (pin 4) gives cycle by cycle over current protection. This is accomplished with an internal comparator which compares the voltage generated by the switch current and R_{SENSE} to an internal reference. In the NCP1606A, this reference is 1.7 V (typ). The NCP1606B has a reduced OCP threshold of 0.5 V (typ) for improved R_{SENSE} power dissipation.

Pin 5 (ZCD) senses the demagnetization of the boost inductor. The next driver on time begins when the voltage at this pin rises above 2.1 V (typ) and then drops below about 1.6 V (typ). A resistor from the zero current detection (ZCD)

winding limits the current into this pin. Additionally, by pulling this pin to ground, the drive pulses are disabled and the controller is placed in a low current standby mode.

The NCP1606 features a powerful output driver on pin 7. This driver is capable of switching the gates of large MOSFETs in an efficient manner. The driver incorporates both active and passive pulldown circuitry to prevent the output from floating high when V_{CC} is off.

Pin 8 (V_{CC}) powers the controller. When V_{CC} is below its turn on level ($V_{CC(on)}$, typically 12 V), the current consumption of the part is limited to < 40 μA. This gives excellent startup times and reduces standby power losses. Alternatively, V_{CC} can also be directly supplied from another controller, such as the NCP1230. This approach can further improve standby power performance in a two stage SMPS system.

For detailed information on the operation of the NCP1606, please refer to NCP1606/D at www.onsemi.com.

Design Procedure

The design of a CRM Boost PFC circuit has been discussed in many ON Semiconductor application notes (see Table 1). This application note will briefly go through the design procedure for a 400 V, 100 W converter using the features of the NCP1606. A design aid, which gives these equations and results, is available at www.onsemi.com.

Table 1.

AND8123	Power Factor Correction Stages Operating in Critical Conduction Mode
AND8016	Design of Power Factor Correction Circuits Using the MC33260
AND8154	NCP1230 90 W, Universal Input Adapter Power Supply with Active PFC
HBD853	Power Factor Correction Handbook

*Additional resources for the design and understanding of CRM Boost PFC circuits available at www.onsemi.com.

DESIGN STEP 1: Define the Required Boost Parameters

Minimum AC Line Voltage	Vac_{LL}	88	V_{RMS}
Maximum AC Line Voltage	Vac_{HL}	264	V_{RMS}
Line Frequency	f_{LINE}	47−63	Hz
Boost PFC Output Voltage	V_{OUT}	400	V
Maximum Output Voltage	$V_{OUT(max)}$	440	V
Boost Output Power	P_{OUT}	100	W
Minimum Switching Frequency	$f_{SW(min)}$	50	kHz
Estimated Efficiency	η	92	%

DESIGN STEP 2: Calculate the Boost Inductor

The boost inductor is calculated with Equation 1:

$$L = \frac{Vac^2 \cdot \left(\frac{V_{OUT}}{\sqrt{2}} - Vac\right) \cdot \eta}{V_{OUT} \cdot P_{OUT} \cdot f(min) \cdot \sqrt{2}} \qquad \text{(eq. 1)}$$

To ensure the required minimum switching frequency, the boost inductor must be evaluated at both the minimum and maximum RMS line voltage. This results gives:

- L @ 88 Vrms = 491 μH
- L @ 264 Vrms = 427 μH

A value of 390 μH was selected. Equation 2 can be used to calculate the resultant minimum frequency at full load.

$$f_{SW} = \frac{Vac^2 \cdot \eta}{2 \cdot L \cdot P_{OUT}} \cdot \left(1 - \frac{Vac \cdot \sqrt{2}}{V_{OUT}}\right) \qquad \text{(eq. 2)}$$

This gives 63 kHz at 88 Vrms and 55 kHz at 264 Vrms.

DESIGN STEP 3: Size the Ct Capacitor

The Ct capacitor must be large enough to accommodate the maximum on time at low line and full power. The maximum on time is given by:

$$T_{ON(max)} = \frac{2 \cdot L \cdot P_{OUT}}{\eta \cdot Vac_{LL}^2} = 11.0\ \mu s \qquad \text{(eq. 3)}$$

However, delivering too long an on time allows the application to deliver excessive power and also reduces the control range at high line or light loads. Therefore, the Ct cap is best sized slightly larger then that given by Equation 4:

$$Ct > \frac{I_{charge} \cdot T_{ON(max)}}{V_{CT(max)}} = \frac{2 \cdot P_{OUT} \cdot L \cdot I_{charge}}{\eta \cdot Vac_{RMS}^2 \cdot V_{CT(max)}} \qquad \text{(eq. 4)}$$

Where I_{charge} and $V_{CT(MAX)}$ are found in the NCP1606 datasheet. To ensure that the maximum on time can always be delivered, use the maximum I_{charge} and the minimum $V_{CT(MAX)}$ in the calculations for Ct. From the NCP1606 datasheet:

- $V_{CT(MAX)}$ = 2.9 V (min)
- I_{charge} = 297 μA (max)

This gives a Ct value of 1.1 nF. A normalized value of 1.2 nF (±10%) gives enough margin.

DESIGN STEP 4: Determine the ZCD Turns Ratio

A winding taken off of the boost inductor gives the zero current detection (ZCD) information. When the switch is on, the ZCD voltage is equal to:

$$V_{ZCD(on)} = \frac{-V_{in}}{N_B : N_{ZCD}} \quad \text{(eq. 5)}$$

where V_{in} = the instantaneous AC line voltage

When the switch is off, the ZCD voltage is equal to:

$$V_{ZCD(off)} = \frac{V_{OUT} - V_{in}}{N_B : N_{ZCD}} \quad \text{(eq. 6)}$$

To activate the zero current detection comparators of the NCP1606 (see Figure 5), the ZCD turns ratio must be sized such that at least V_{ZCDH} (2.1 V typ) is obtained on the ZCD pin during all operating conditions. This means that:

$$N_B : N_{ZCD} \leq \frac{V_{OUT} - Vac_{HL} \cdot \sqrt{2}}{V_{ZCDH}} = 11.6 \quad \text{(eq. 7)}$$

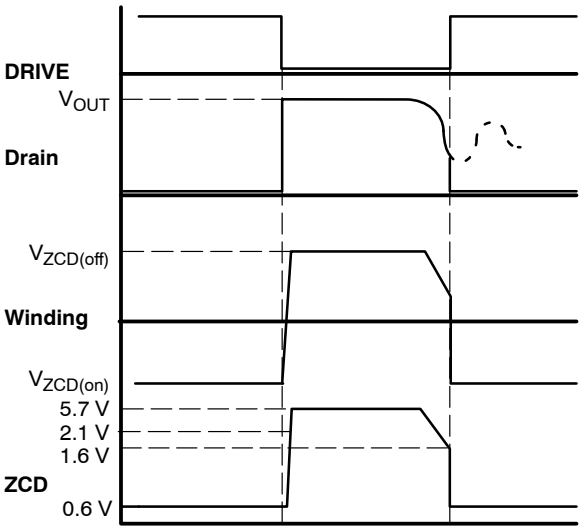

Figure 4. Voltage Waveforms for Zero Current Detection

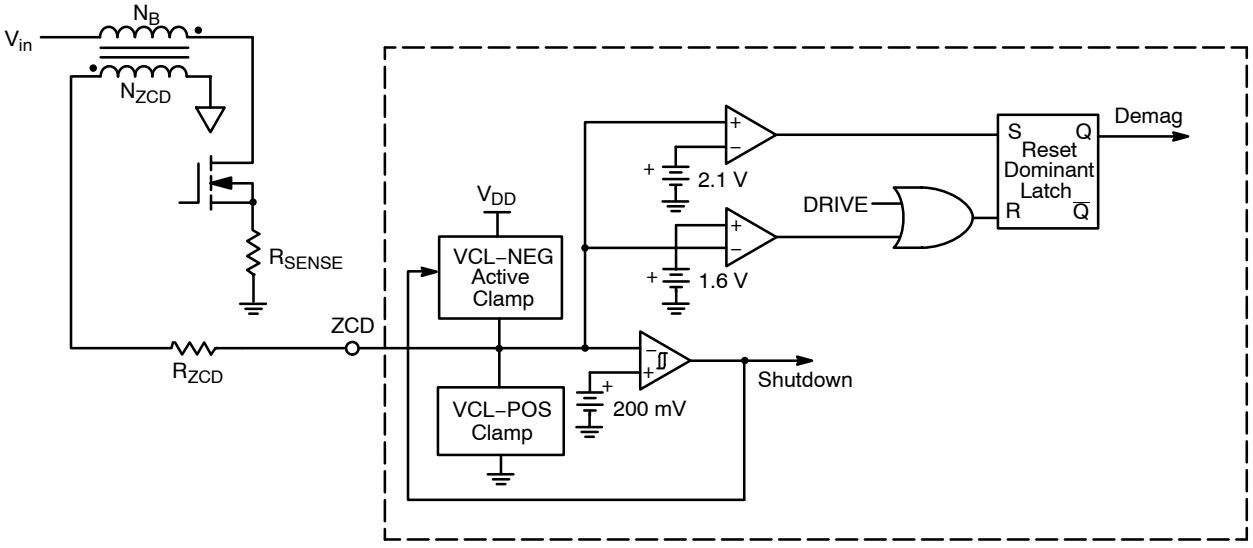

Figure 5. ZCD Winding and Internal Logic Arrangement

A turns ratio of 10 was selected for this design. A resistor, R_{ZCD}, is added between the ZCD winding and pin 5 to limit the current into or out of the pin. This current must be low enough so as to not trigger the ZCD shutdown feature. Therefore, R_{ZCD} must be:

$$R_{ZCD} \geq \frac{Vac_{HL} \cdot \sqrt{2}}{I_{CL\_NEG} \cdot (N_B : N_{ZCD})} = 14.9\ k\Omega \quad \text{(eq. 8)}$$

where I_{CL_NEG} = 2.5 mA (from the NCP1606 datasheet)

However, the value of this resistor and the small parasitic capacitance of the ZCD pin also determines when the ZCD winding information is detected and the next drive pulse begins. Ideally, the ZCD resistor will restart the drive at its valley. This will minimize switching losses by turning the MOSFET back on when its drain voltage is at a minimum. The value of R_{ZCD} to accomplish this is best found experimentally. Too high of a value could create a significant delay in detecting the ZCD event. In this case, the controller would operate in discontinuous conduction mode (DCM) and the power factor would suffer. Conversely, if the ZCD resistor is too low, then the next driver pulse would start when the voltage is still high and switching efficiency would suffer.

DESIGN STEP 5: Set the FB, OVP, and UVP Levels

Because of the slow bandwidth of the PFC stage, the output can suffer from overshoots during transient loads or at startup. To prevent this, the NCP1606 incorporates an adjustable overvoltage protection (OVP) circuit. The OVP activation level is set by R_{OUT1}. A derivation in the NCP1606 datasheet shows that:

$$V_{OUT(max)} = V_{OUT(nom)} + R_{OUT1} \cdot I_{OVP} \quad \text{(eq. 9)}$$

where I_{OVP} = 40 μA (for NCP1606A)

or I_{OVP} = 10 μA (for NCP1606B)

Therefore, to achieve the desired maximum output voltage with the NCP1606B, R_{OUT1} is equal to:

$$R_{OUT1} = \frac{V_{OUT(max)} - V_{OUT(nom)}}{I_{OVP}} \quad \text{(eq. 10)}$$

This gives a value of 4.0 MΩ for the NCP1606B or 1.0 MΩ for the NCP1606A.

R_{OUT2} is then sized to maintain 2.5 V on the FB pin when Vout is at its targeted level.

$$R_{OUT2} = \frac{2.5\ V \cdot R_{OUT1}}{V_{OUT(nom)} - 2.5\ V} \quad \text{(eq. 11)}$$

This gives a value of 25.2 kΩ for the B version or 6.3 kΩ for the A version.

When determining the maximum output voltage level, care must be exercised so as not to interfere with the natural line frequency ripple on the output capacitor. This ripple is caused by the averaging effect of the PFC stage: the current charging the bulk cap is sinusoidal and in phase with the input line, but the load current is not. The resultant ripple voltage can be calculated as:

$$Vripple_{(pk-pk)} = \frac{P_{OUT}}{C_{bulk} \cdot 2 \cdot \pi \cdot f_{LINE} \cdot V_{OUT}} \quad \text{(eq. 12)}$$

where f_{LINE} = 47 Hz (worst case for ripple)

A bulk capacitor value of 68 μF gives a peak to peak ripple of 12.5 V. This is well below the peak output overvoltage level (40 V).

The NCP1606 also incorporates undervoltage protection (UVP). Under normal conditions, the boost output capacitor will charge to the peak of the ac line. But if it does not charge to some minimum voltage, then the NCP1606 enters undervoltage protection. The minimum output voltage that must be sensed is given by:

$$Vout_{UVP} = \frac{R_{OUT1} + R_{OUT2}}{R_{OUT2}} \cdot V_{UVP} = 48.0\ V \quad \text{(eq. 13)}$$

where V_{UVP} = 300 mV (typ)

Note that this feature also provides protection against open loop conditions in the feedback path. Consider that if R_{OUT1} was inadvertently open (perhaps due to a bad solder joint), the boost application would normally see that the FB pin is too low (0 V in this case) and respond by delivering maximum power. This could raise the output voltage well above its maximum, potentially causing catastrophic results. However, the NCP1606 incorporates a novel feature which waits 180 μs at startup prior to issuing the first drive pulse. Since the built in error amplifier would normally pull FB to 2.5 V, the NCP1606 leaves the error amplifier disabled during this time. If the FB pin is less than the UVP level (300 mV), it continues to disable both the driver output and the error amplifier. Thus, an undervoltage or open loop condition can be always be accurately detected at startup (Figure 6).

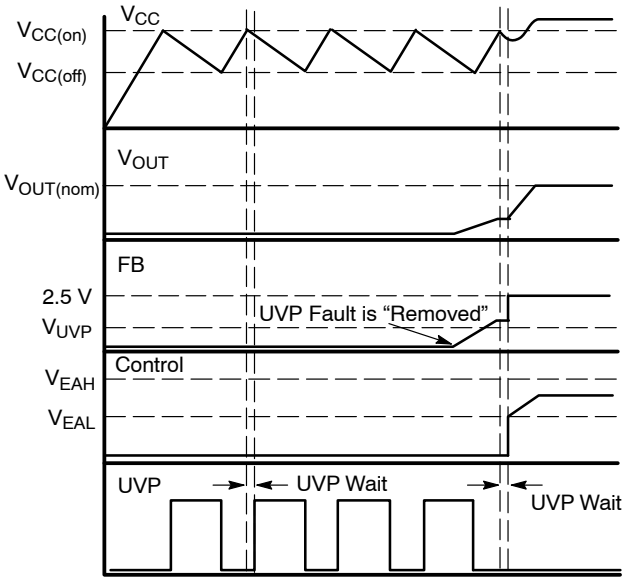

Figure 6. Timing Diagram Showing UVP and Recovery from UVP

If the open loop event occurs after startup, then the fault may not be detected immediately. This is because the error amplifiers regulates the control pin to achieve 2.5 V on the FB pin. Therefore, the FB voltage can only drop once the maximum control pin voltage is achieved. When the FB voltage drops below the UVP threshold, then the undervoltage fault will be entered. The situation is depicted in Figure 7.

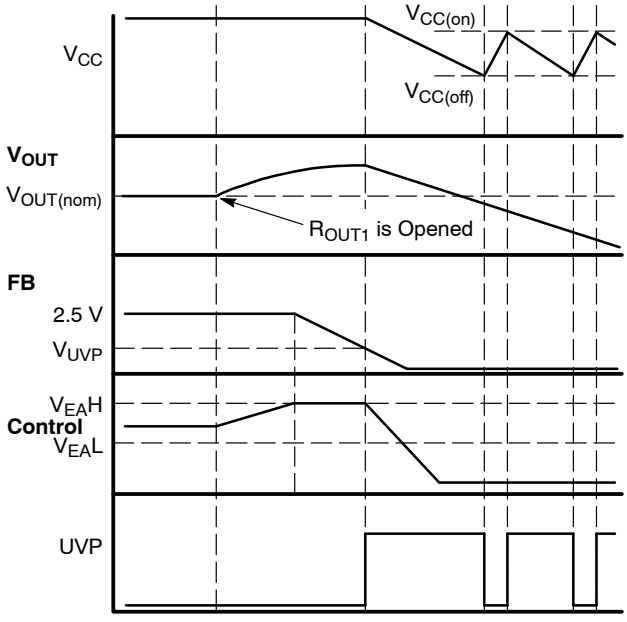

Figure 7. UVP Operation if R_{OUT1} is Opened After Startup

DESIGN STEP 6: Size the Power Components

The power components must be properly sized for the necessary current and voltages which they will experience. The stresses are greatest at full load and low line.

1. The Boost inductor, L

$$I_{L(peak)} = \frac{2 \cdot \sqrt{2} \cdot P_{OUT}}{\eta \cdot Vac_{LL}} = 3.49\ A \quad \text{(eq. 14)}$$

$$Icoil_{RMS} = \frac{2 \cdot P_{OUT}}{\sqrt{3} \cdot Vac_{LL} \cdot \eta} = 1.43\ A \quad \text{(eq. 15)}$$

2. The Boost Diode, D_{BOOST}

$$I_{D(rms)} = \frac{4}{3} \cdot \sqrt{\frac{2 \cdot \sqrt{2}}{\pi}} \cdot \frac{P_{OUT}}{\eta \cdot \sqrt{Vac_{LL} \cdot V_{OUT}}} = 0.73\ A \quad \text{(eq. 16)}$$

3. The MOSFET, M1

$$I_{M(rms)} = \frac{2}{\sqrt{3}} \cdot \left(\frac{P_{OUT}}{\eta \cdot Vac_{LL}}\right) \cdot \sqrt{\left[1 - \left(\frac{8 \cdot \sqrt{2} \cdot Vac_{LL}}{3 \cdot \pi \cdot V_{OUT}}\right)\right]} = 1.22\ A \quad \text{(eq. 17)}$$

The MOSFET will see a maximum voltage equal to the V_{OUT} overvoltage level (440 V for this example). If an 80% derating is used for the MOSFET's BV_{DSS}, then a 550 V FET gives adequate margin.

4. The sense resistor, R_{SENSE}

$$R_{SENSE} = \frac{V_{CS(limit)}}{I_{peak}} = 0.14\ \Omega\ (B) \text{ or } 0.49\ \Omega\ (A) \quad \text{(eq. 18)}$$

$$P_{Rsense} = I_{M(rms)}{}^2 \cdot R_{SENSE} = 0.21\ W\ (B) \text{ or } 0.73\ W\ (A) \quad \text{(eq. 19)}$$

$V_{CS(limit)}$ = 0.5 V (typ) for the NCP1606B; $V_{CS(limit)}$ = 1.7 V (typ) for the NCP1606A

5. The bulk capacitor, C_{BULK}

$$I_{C(rms)} = \sqrt{\frac{32 \cdot \sqrt{2} \cdot P_{OUT}{}^2}{9 \cdot \pi \cdot Vac_{LL} \cdot V_{OUT} \cdot \eta^2} - (I_{LOAD(rms)})^2} = 0.69\ A \quad \text{(eq. 20)}$$

The bulk cap value was calculated in Step 5 to give an acceptable ripple voltage which would not trigger the output over voltage protection. This value may need to be further increased so as to give an RMS current that is within the capacitor's ratings.

The voltage rating of the bulk cap should be greater than the maximum V_{OUT} level. Since this design has an output overvoltage level of 440 V, a 450 V capacitor was selected.

DESIGN STEP 7: Supply V_{CC}

Generally, a resistor connected between the ac input and pin 8 charges up the V_{CC} cap to the $V_{CC(on)}$ level. Because of the very low consumption of the NCP1606 during this stage, most of the current goes directly to charging up the V_{CC} cap. This provides faster startup times and reduced standby power dissipation. The startup time can be approximated with the following equation:

$$T_{start} = \frac{C_{Vcc} \cdot V_{CC(on)}}{\frac{Vac_{(rms)} \cdot \sqrt{2}}{R_{start}} - I_{CC(startup)}} \quad \text{(eq. 21)}$$

where $I_{CC(startup)}$ = 40 μA (max)

When the V_{CC} voltage exceeds the $V_{CC(on)}$ level (12 V typical), the internal references and logic of the NCP1606 turn on. The controller has an undervoltage lockout (UVLO) feature which keeps the part active until V_{CC} drops below about 9.5 V. This hysteresis allows ample time for another supply to take over and provide the necessary power to V_{CC}. The ZCD winding is an excellent candidate, but the voltage generated on the winding can be well below the desired V_{CC} level. Therefore, a small charge pump must be constructed to supply V_{CC}. Such a schematic is illustrated in Figure 8.

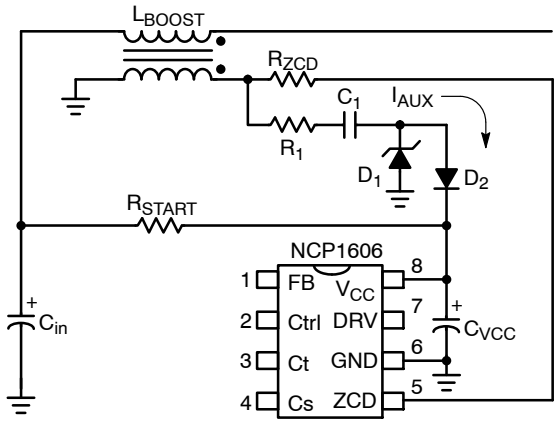

Figure 8. The ZCD Winding can Supply V_{CC} through a Charge Pump Circuit

C1 stores the energy for the charge pump. R1 limits the current by reducing the rate of voltage change. D1 supplies current to C1 when its cathode is negative. When its cathode is positive it limits the maximum voltage applied to V_{CC}. When the ZCD winding is switching, the voltage change across C1 over one period is:

$$\Delta V_{C1} = \frac{V_{OUT} - V_{CC}}{N : N_{ZCD}} \quad \text{(eq. 22)}$$

Therefore, the current available for charging V_{CC} is:

$$I_{AUX} = C1 \cdot f_{SW} \cdot \Delta V_{C1} = C1 \cdot f_{SW} \cdot \frac{V_{OUT} - V_{CC}}{N : N_{ZCD}} \quad \text{(eq. 23)}$$

For off line ac−dc applications which require PFC, a 2 stage approach is generally used. The first stage is the CRM boost PFC. This supplies the 2nd stage−−traditionally an isolated flyback or forward converter. This solution can exhibit excellent performance at a low cost. However, during light load operations, the input current is low and the PFC stage is not necessary. In fact, leaving it on only degrades the efficiency of the system. Advanced controllers, such as the NCP1230 and NCP1381, can detect this light load case and instruct the PFC to shut down (Figure 9). The

NCP1606 is compatible with this type of topology, provided that the supplied V_{CC} is initially greater than the NCP1606's $V_{CC(on)}$ level.

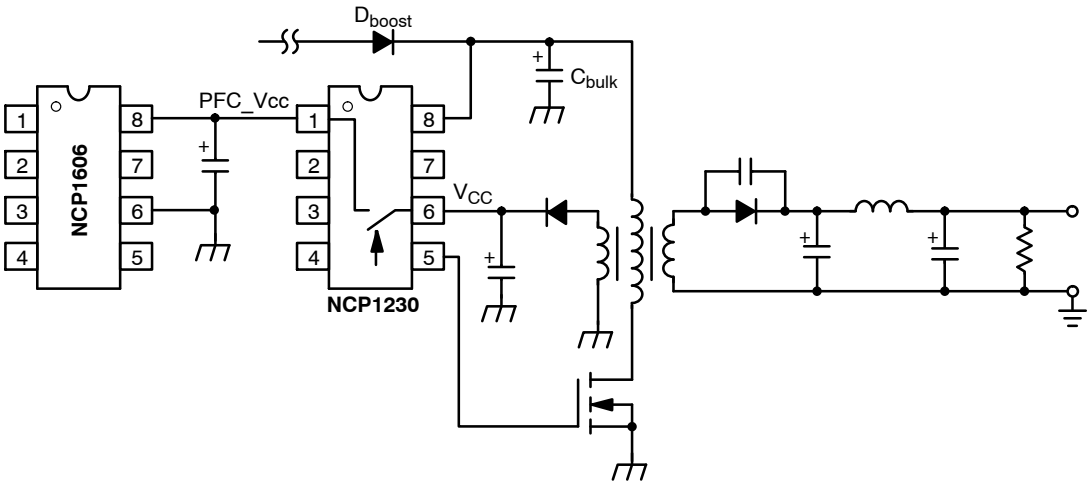

Figure 9. Using the SMPS Controller to Supply Power to the NCP1606

DESIGN STEP 8: Limit the Inrush Current

The sudden application of the mains to the PFC converter can cause the circuit to experience an inrush current and a resonant voltage overshoot that is several times normal values. To resize the power components to handle this is cost prohibitive. Furthermore, the controller cannot do anything to protect against this. Turning on the boost switch would only make the issue worse. There are two primary ways to solve this issue:

1. Startup Bypass Rectifier

A rectifier can be added from the input voltage to the output voltage (Figure 10). This bypasses the inductor and diverts the startup current directly to the bulk capacitor. The bulk capacitor is then charged to the peak ac line voltage without resonant overshoot and without excessive inductor current. After startup, D_{BYPASS} will be reverse biased and will not interfere with the boost converter.

2. External Inrush Current Limiting Resistor

An NTC (negative temperature coefficient) thermistor in series with the boost inductor can limit the inrush current (Figure 11). The resistance value drops from a few ohms to a few milliohms as the device is heated by the I^2R power dissipation. Alternatively, this NTC can be placed in series with the boost diode. This improves the active efficiency as the resistor only sees the output current instead of the input current. However, an NTC resistor may not be able to adequately protect the inductor and bulk capacitor against inrush current during a brief interruption of the mains, such as during line drop out and recovery.

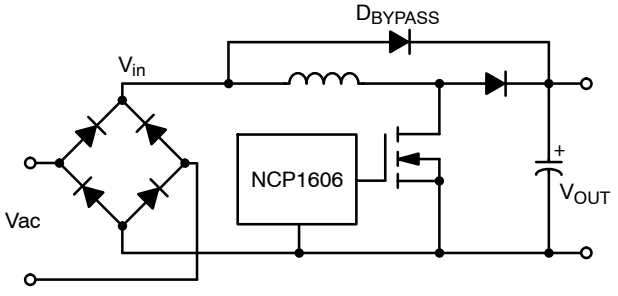

Figure 10. Use a Second Diode to Route the Inrush Current Away from the Inductor

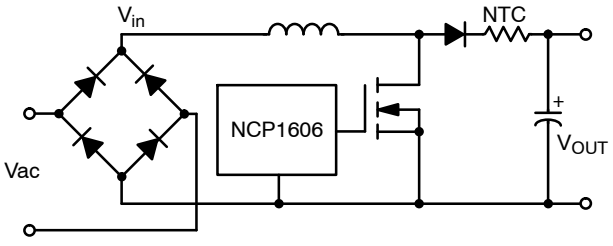

Figure 11. Use an NTC to Limit the Inrush Current Through the Inductor

DESIGN STEP 9: Develop the Compensation Network

As stated earlier, due to the natural output voltage ripple, the bandwidth of the PFC feedback loop is generally kept below 20 Hz. For a simple type 1 compensation network, only a capacitor is placed between FB and Control. The gain, G(s), of the feedback network is then given by:

$$G(s) = \frac{1}{s \cdot R_{OUT1} \cdot C_{COMP}} \quad \text{(eq. 24)}$$

Therefore, the capacitor necessary to attenuate the bulk voltage ripple is given by:

$$C_{COMP} = \frac{10^{G/20}}{4 \cdot \pi \cdot f_{LINE} \cdot R_{OUT1}} \quad \text{(eq. 25)}$$

where G is the attenuation level in dB (commonly 60 dB) and f_{LINE} is the minimum AC line frequency (47 Hz).

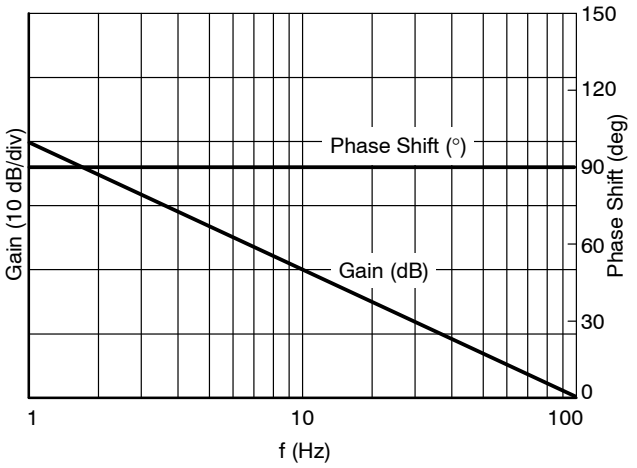

Figure 12. Gain and Phase for a Type 1 Feedback Network

As shown in Figure 12, a type 1 compensation network provides no phase boost to improve stability. For resistive loads, this may be sufficient (Figure 13). But for constant power loads, such as SMPS stages, the phase margin can suffer (Figure 14).

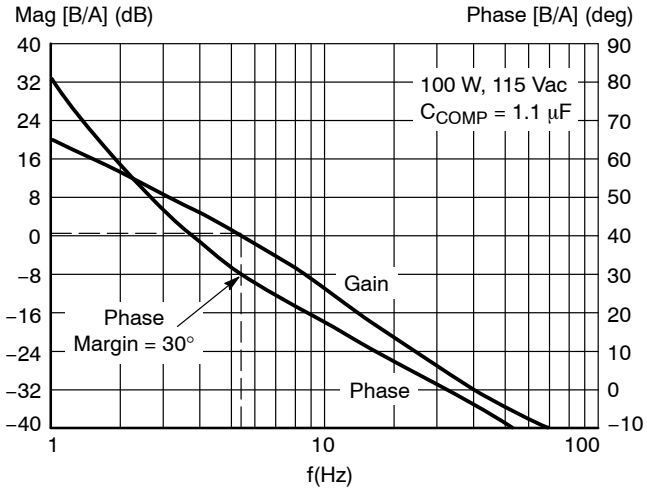

Figure 13. Boost demo board with a resistive load. Phase margin = 30 deg.

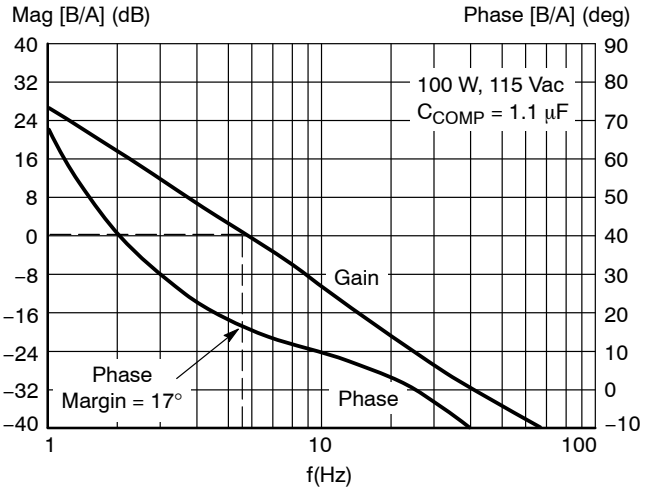

Figure 14. Boost demo board with a constant power load. Phase margin has been reduced to 17 deg.

If greater system stability is required, then a type 2 compensation network can be implemented. In this setup, a resistor and capacitor are placed in parallel with C_{COMP} (Figure 15).

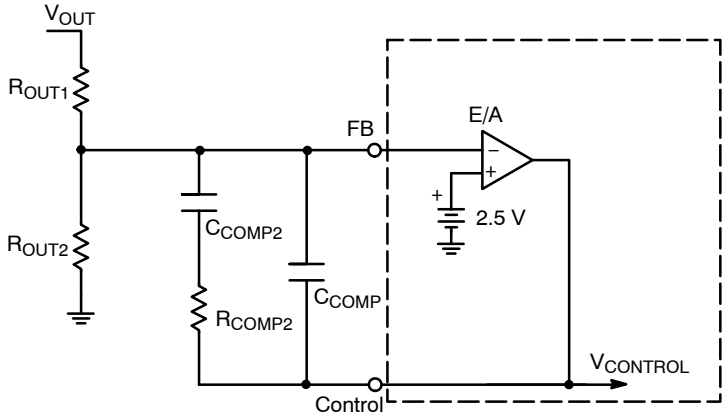

Figure 15. Type 2 compensation network

The transfer function for the error amplifier is now:

$$G(s) = \frac{1 + s \cdot R_{COMP2} \cdot C_{COMP2}}{s \cdot R_{OUT1} \cdot (C_{COMP} + C_{COMP2}) \cdot \left(1 + s \cdot R_{COMP2} \cdot \left(\frac{C_{COMP} \cdot C_{COMP2}}{C_{COMP} + C_{COMP2}}\right)\right)} \quad \text{(eq. 26)}$$

This gives a pole at 0 Hz, a zero at f_Z (eq 27), and another pole at f_P (eq 28).

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_{COMP2} \cdot C_{COMP2}} \quad \text{(eq. 27)}$$

$$f_P = f_Z \cdot \left(\frac{C_{COMP} + C_{COMP2}}{C_{COMP}}\right) \quad \text{(eq. 28)}$$

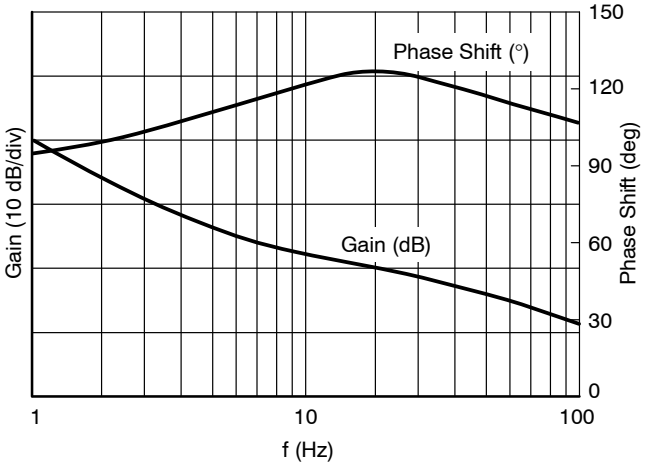

Figure 16. Representative Gain and Phase for a Type 2 Feedback Network. Note the Phase Boost

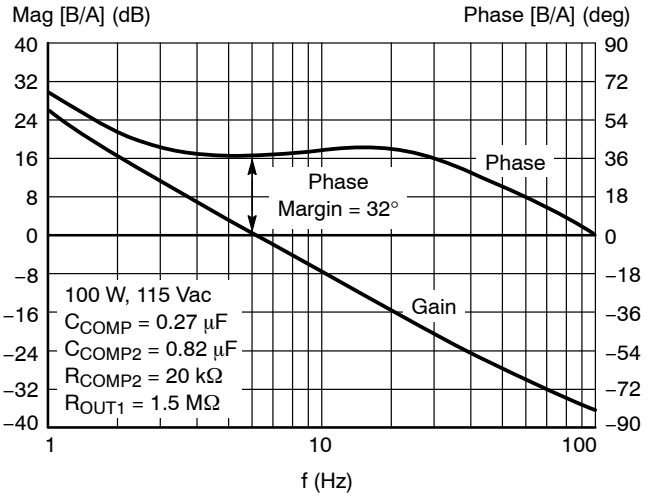

Figure 17. Improved Stability with a Type 2 Compensation Network. Phase Margin = 32 deg.

The poor stability observed with the type 1 compensation in Figure 14 has now been improved (with the same total compensation capacitance) to Figure 17.

The phase margin and cross over frequency will change with the line voltage. Therefore, it is critical that any design has the gain−phase measured under all operating conditions. This can be accomplished with a simple setup (Figure 18) and a good network analyzer.

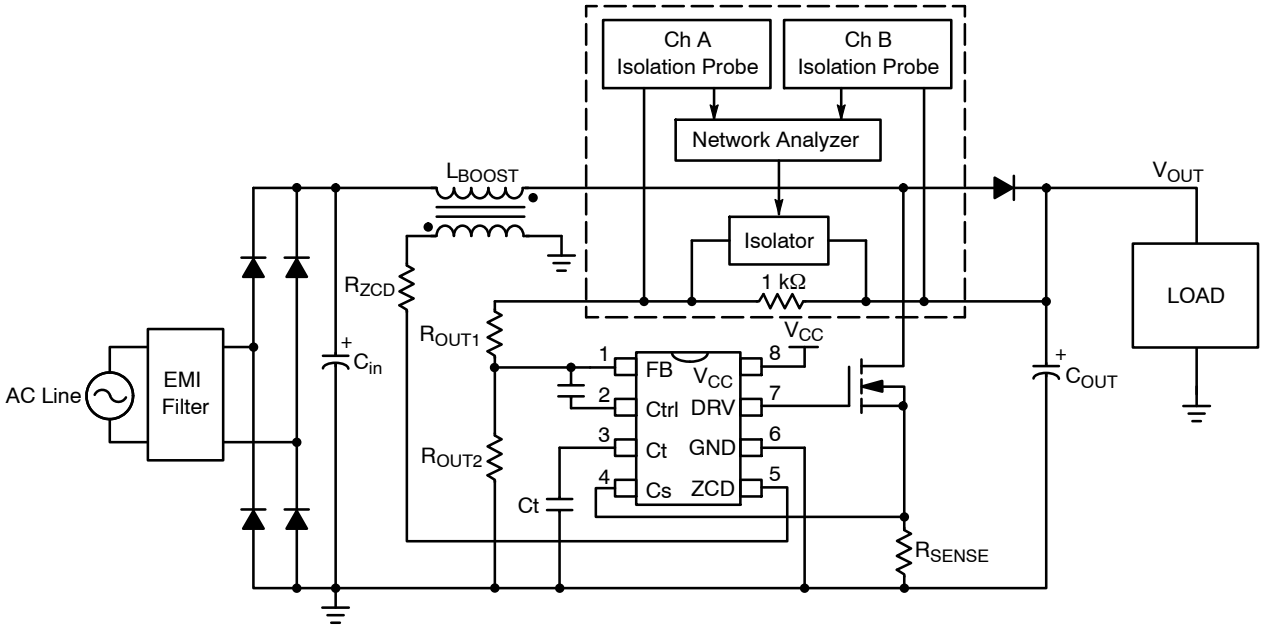

Figure 18. Gain−Phase Measurement Setup for Boost PFC Pre−converters

Simple Improvements for Additional THD Reduction

The NCP1606, with its constant on time architecture, gives a good deal of flexibility in optimizing each design. If further power factor performance is necessary, consider the following design guidelines.

1. Improve the THD/PF at Full Load by Increasing the On Time at the Zero Crossing:

One issue with CRM control is that at the zero crossing of the AC line, the voltage is not large enough to significantly charge the boost inductor during the fixed on time. Hence, very little energy is processed and some “zero crossover distortion” (Figure 19) may be produced.

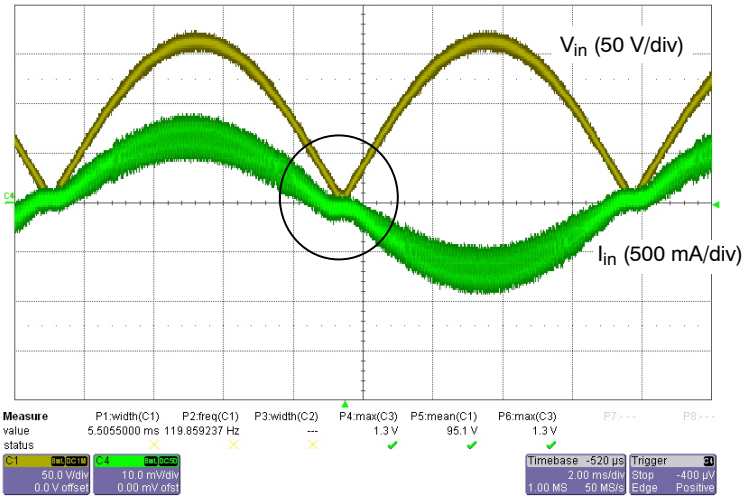

Figure 19. Zero Crossover Distortion

This lowers the THD and PF of the pre−converter. To meet IEC1000 requirements, this is generally not an issue, as the NCP1606 delivers more than an ample reduction in current distortion. However, if improved THD or PF is required, then this zero crossover distortion can be reduced. The key is to increase the on time when the input voltage is low. This allows more time for the inductor to charge up and reduces the voltage level at which the distortion begins.

Fortunately, such a method is easy to implement on the NCP1606. If a resistor was tied from pin 3 (Ct) to the input voltage, then a current proportional to the instantaneous line voltage would be injected into the capacitor (Figure 20). This current would be much higher at the peak of the line and have nearly no effect at low input voltages.

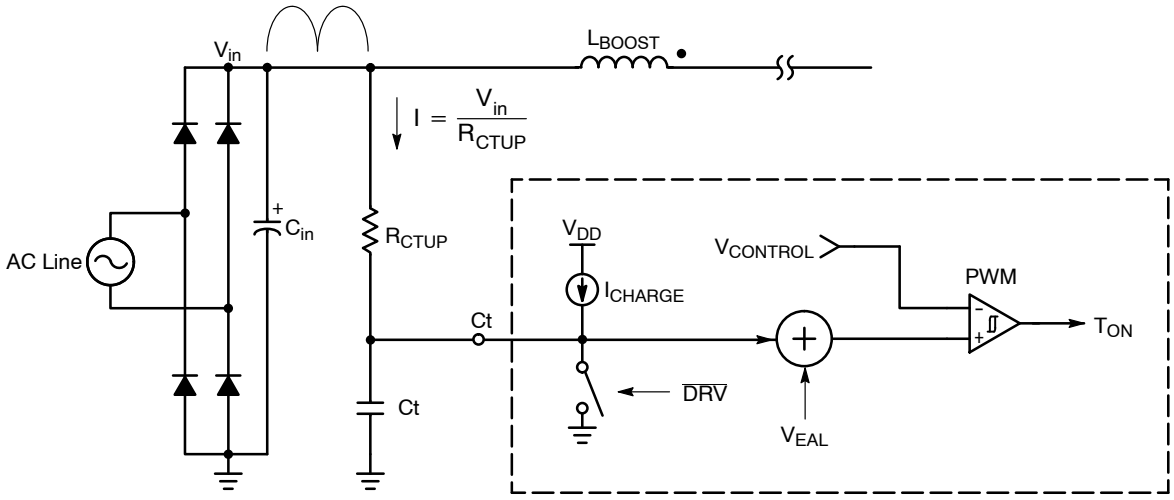

Figure 20. Add R_{CTUP} to Modify the On Time and Reduce the Zero Crossing Distortion

Therefore, the Ct capacitor can be increased in size so that the on time is a little longer near the zero crossing (Figure 21). This also reduces the frequency variation over the ac line cycle. The disadvantage to this approach is the increased no load power dissipation created by R_{CTUP}. The designer must balance the desired THD and PF performance with the no load power dissipation requirements.

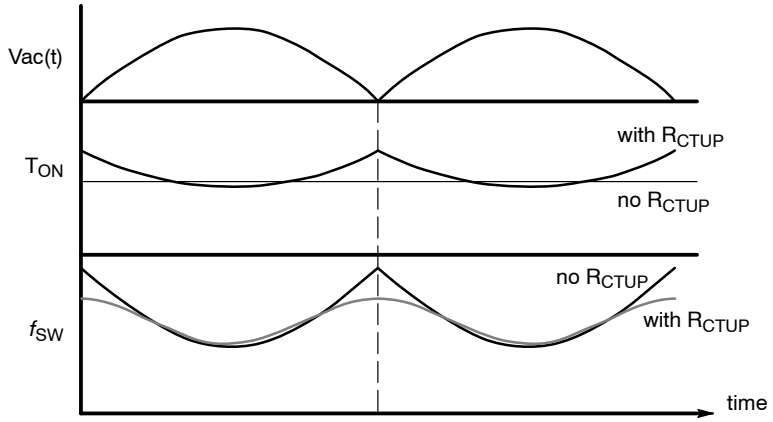

Figure 21. On Time and Switching Frequency With and Without R_{CTUP}

The effect of this resistor on THD and power factor is illustrated in Figure 22.

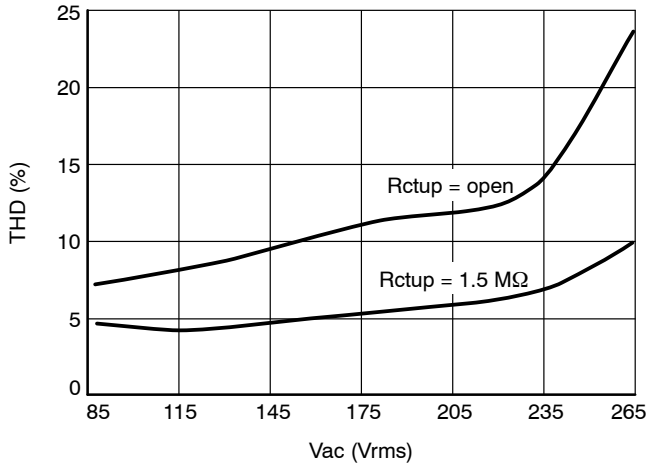

Figure 22. Effect of Rctup on Full Load (100 W) THD

2. Improve the THD/PF at Light Load or High Line:

If the required on time at light load or high line is less than the minimum on time, then the controller will deliver too much power. Eventually, this will cause the control voltage to fall to its lowest level (V_{EAL}). The controller will then disable the drive (static OVP) to prevent the output voltage from rising too high. Once the output drops lower, the control voltage will rise and the cycle will repeat. Obviously, this will add to the distortion of the input current and output voltage ripple. However, there are two simple solutions to remedy the problem:

1. Properly size the Ct capacitor. As mentioned above, the capacitor must be large enough to deliver the required on time at full load and low line. However, sizing it too large means that the range of control levels at light power will be reduced. And as the Ct capacitor becomes larger, the minimum on time of the driver will also increase.
2. Compensate for propagation delays. If optimizing the Ct capacitor still does not achieve the desired performance, then it may be necessary to compensate for the propagation delay. When the Ct voltage exceeds the $V_{CONTROL}$ setpoint, the PWM comparator sends a signal to end the on time of the driver (Figure 23).

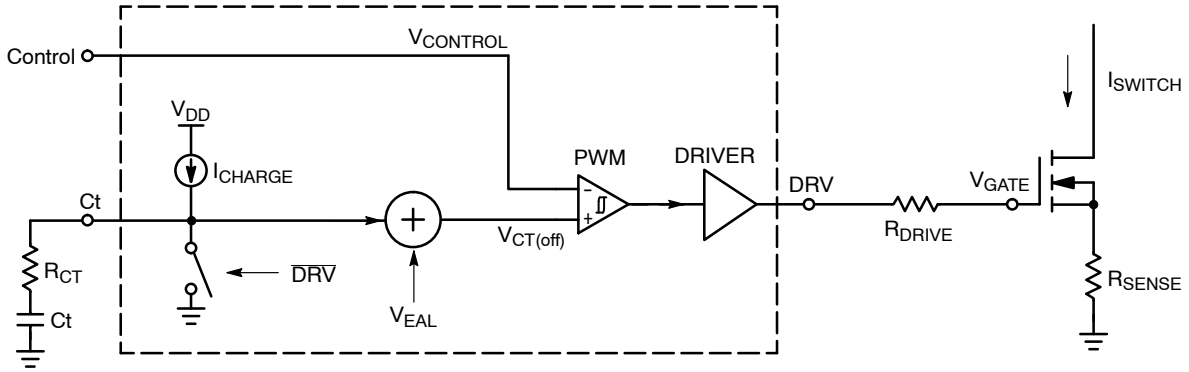

Figure 23. Block Diagram of the Propagation Delay Components

However, there is some delay before the MOSFET fully turns off. This delay is created by the propagation delay of the PWM comparator and the time to bring the MOSFET's gate voltage to zero (Figure 24).

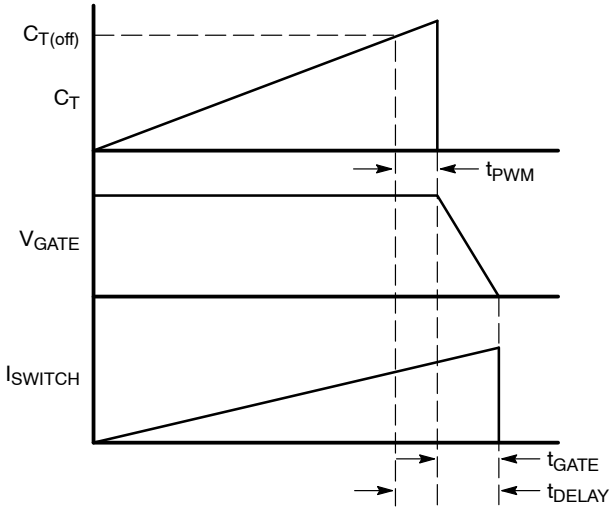

Figure 24. Driver Turn Off Propagation Delay

The total delay, t_{DELAY}, is summarized in eq 29:

$$t_{DELAY} = t_{PWM} + t_{GATE} \quad \text{(eq. 29)}$$

This delay adds to the effective on time of the controller. But if a resistor (R_{CT}) is inserted in series with the Ct capacitor, then the total on time is reduced by:

$$\Delta t = Ct \cdot \frac{\Delta V_{RCT}}{\Delta I_{RCT}} = Ct \cdot R_{CT}$$

Therefore, to compensate for the propagation delay, R_{CT} must be:

$$R_{CT} = \frac{t_{DELAY}}{Ct} \quad \text{(eq. 30)}$$

The NCP1606 datasheet gives a typical t_{PWM} of 100 ns. The t_{GATE} delay is a function of the MOSFET's gate charge and the resistor "R_{DRIVE}." For this demo board, the gate delay was measured at about 150 ns. Therefore, a value of R_{CT} = 300 Ω is sufficient to compensate for the propagation delays. This can improve PF and THD, particularly at light load and high line (Figure 25).

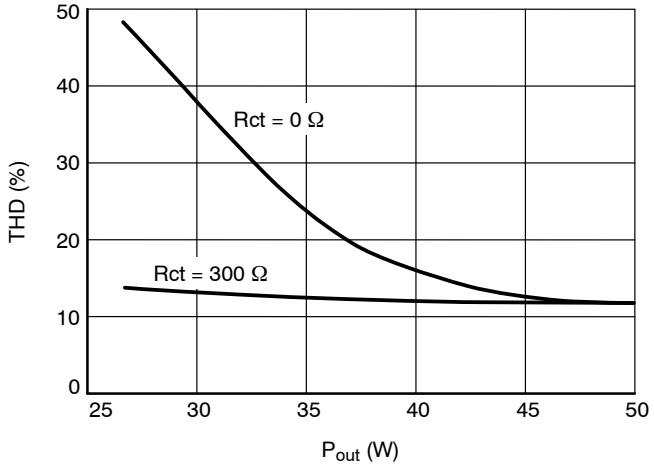

Figure 25. Effect of Rct on Light Load THD at 264 Vac / 50 Hz (Rctup = open)

Design Results

The completed demo board schematic using the NCP1606B is shown in Figure 26.

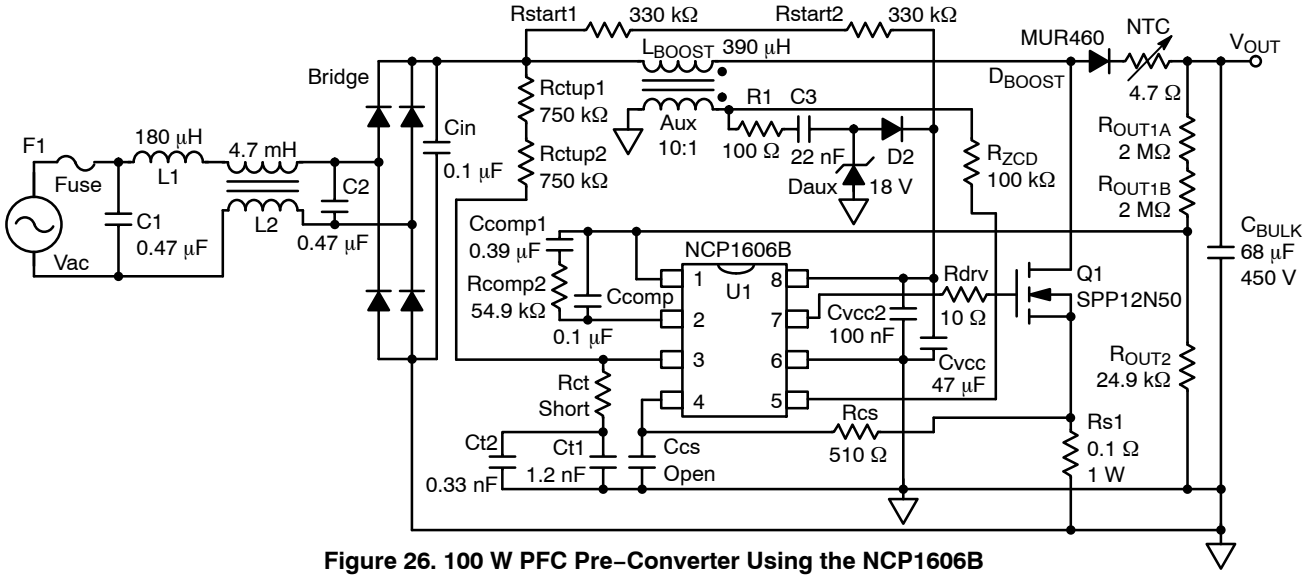

Figure 26. 100 W PFC Pre−Converter Using the NCP1606B

The bill of materials (BOM) and layout drawings are shown in Appendix 1 and 2, respectively. This pre−converter exhibits excellent THD (Figure 27), PF (Figure 28), and efficiency (Figure 29).

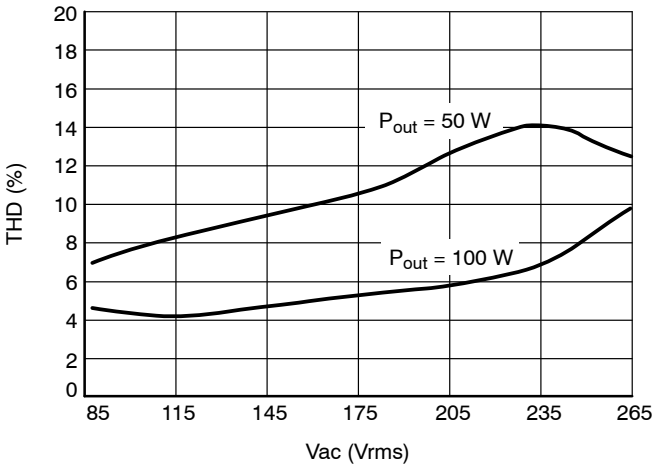

Figure 27. THD vs. Input Voltage at Full Load and 50% Load

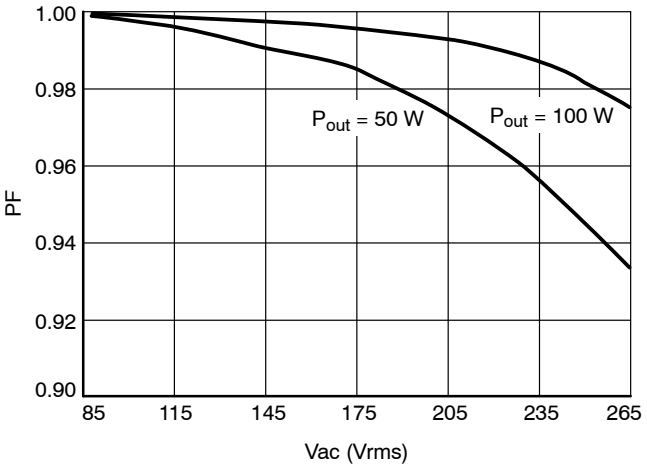

Figure 28. PF vs. Input Voltage at Full Load and 50% Load

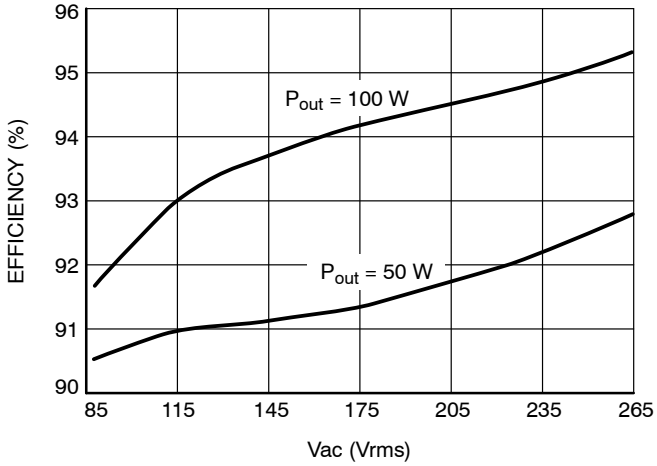

Figure 29. Efficiency vs. Input Voltage at Full Load and 50% Load

The input current and resultant output voltage ripple is shown in Figure 30. The overvoltage protection scheme can be observed by starting up the pre−converter with a light load on the output (Figure 31). The OVP activates at about 440 V and restarts at about 410 V.

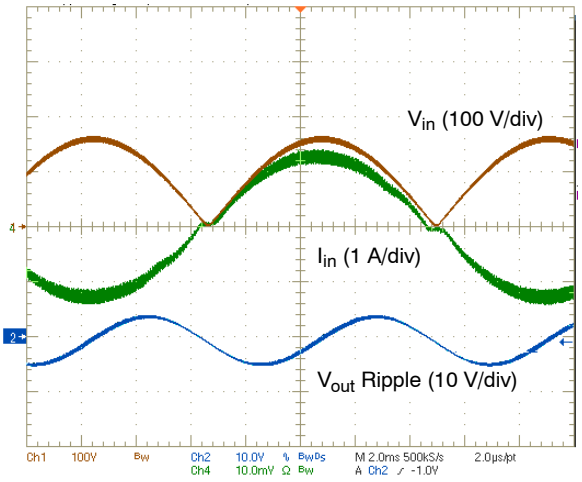

Figure 30. Full Load Input Current at 115 Vac/60 Hz

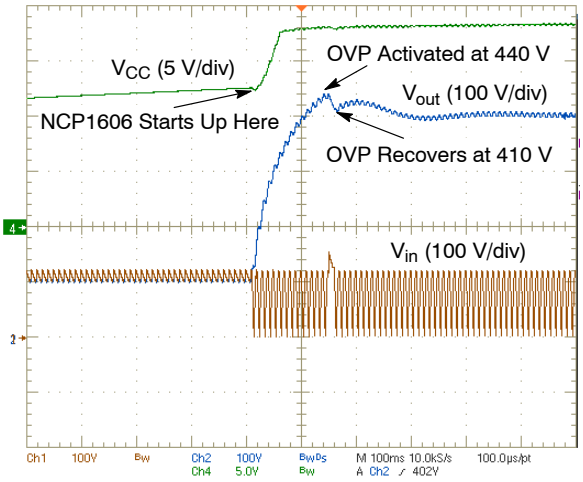

Figure 31. Startup Transient Showing OVP Activation and Recovery

If the NCP1606A is to be used instead, then changes to R_{OUT1}, R_{OUT2}, R_{SENSE}, and the compensation components are necessary. Figure 32 shows the schematic of the 100 W board for the NCP1606A. The changes are highlighted in red.

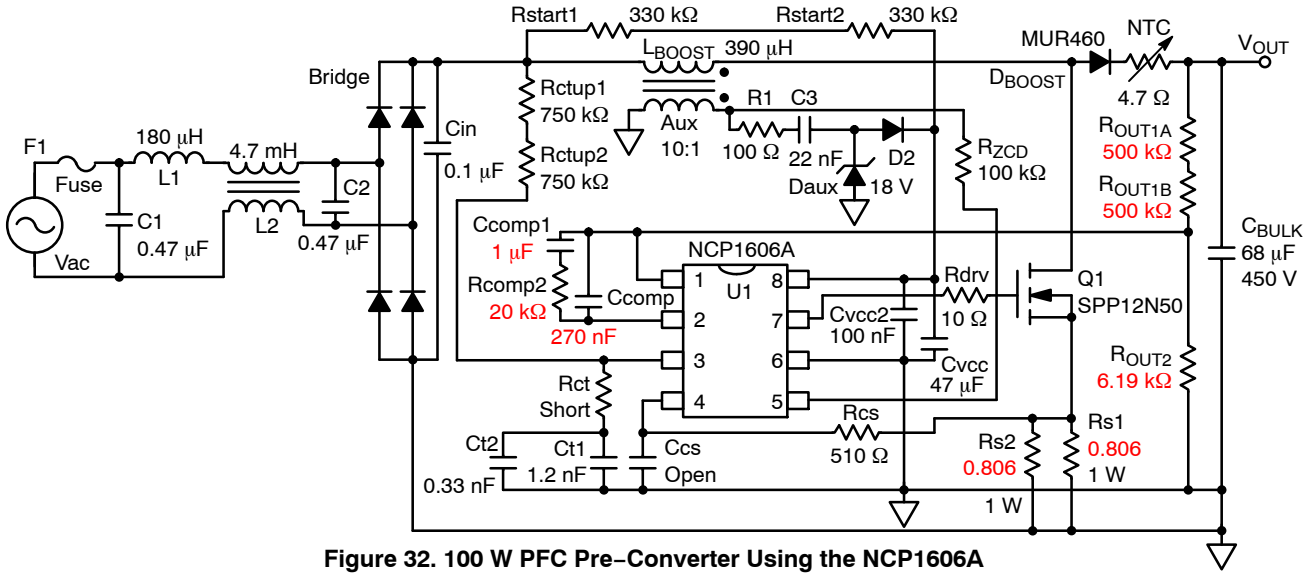

Figure 32. 100 W PFC Pre−Converter Using the NCP1606A

This demo board can be configured in a variety of ways to optimize performance. Table 2 gives some results with a few of these configurations. The data confirms that the addition of Rctup has a beneficial effect on the THD. Additionally, the B version exhibits superior standby power dissipation due to its reduced thresholds on I_{OVP}. It also shows improved active mode efficiency at low line. This is because it uses a smaller $V_{CS(limit)}$ level (0.5 V typical), which decreases the R_{sense} power dissipation by about 70%. This reduction in power consumption is most noticeable at low line, where peak currents are the highest.

Table 2. Summary of key parameters for different variations of the demo board.

Version	ROUT1	RCTUP	Ct	Shutdown (V_{ZCD} = 0 V) Pdiss @ 264 Vac	Efficiency @ 100 W		THD @ 100 W	
					115 Vac 60 Hz	230 Vac 50 Hz	115 Vac 60 Hz	230 Vac 50 Hz
A	1.0 MEG	open	1.2 nF	321 mW	92.5%	94.9%	8.1%	15.1%
A	1.0 MEG	1.5 MEG	1.5 nF	391 mW	92.5%	94.8%	4.5%	7.4%
B	4.0 MEG	open	1.2 nF	217 mW	93.0%	94.9%	8.0%	13.3%
B	4.0 MEG	1.5 MEG	1.5 nF	288 mW	93.0%	94.8%	3.7%	8.9%

Appendix 1: Bill of Materials (BOM)

Designator	Qty.	Description	Value	Manufacturer	Part #
U1	1	NCP1606B	PDIP	ON Semiconductor	NCP1606B
D1	1	General purpose diode	100 V, SOD123	ON Semiconductor	MMSD4148T1G
Daux	1	Zener diode	18 V, 5%	ON Semiconductor	MMSZ4705T1
Dboost	1	Ultrafast diode	4 A, 600 V	ON Semiconductor	MUR460RLG
Bridge	1	Diode Bridge Rectifier	2 A, 600 V	Vishay	2KBP06M−E4/1
C1, C2	2	X cap	0.47 μF, 275 Vac	EPCOS	B81130C1474M
Cin	1	X cap	0.1 μF, 305 Vac	EPCOS	B32921A2104M
Cbulk	1	Electrolytic Cap, Radial	68 μF, 450 V	Panasonic	ESMG451ELL680MN35S
Cvcc	1	Electrolytic Cap, Radial	47 μF, 25 V	Panasonic	EEU−FC1E470
C3	1	SM 1206 capacitor	22 nF, 10%, 25 V		
Ccomp	1	SM 1206 capacitor	100 nF, 10%, 25 V		
Ccomp2	1	SM 1206 capacitor	390 nF, 10%, 25 V		
Ccs	−	SM 1206 capacitor	open		
Ct1	1	SM 1206 capacitor	1.5 nF, 10%, 25 V		
Cvcc2	1	SM 1206 capacitor	100 nF, 10%, 25 V		
L1	1	Input Inductor	180 μH	Coilcraft	PCV−2−184−05L
L2	1	Line Filter	4.7 mH, 2.7 A	Panasonic	ELF−20N027A
Lboost	1	Boost inductor and ZCD winding	390 μH, 10:1	Coilcraft	FA2890−AL
NTC	1	Inrush current limiter, NTC	4.7 Ω, 20%	EPCOS	B57238S479M
Q1	1	TO−220AB N−CH Power MOSFET	11.6 A, 560 V	Infineon	SPP12N50C3X
R1	1	SM 1206 resistor	100 Ω		
Rcomp2	1	SM 1206 resistor	54.9 kΩ		
Rct	1	SM 1206 resistor	short, 1%		
Ro1a, Ro1b	2	SM 1206 resistor	2 MΩ		
Rout2	1	SM 1206 resistor	24.9 kΩ		
Rdrv	1	SM 1206 resistor	10 Ω		
Rs1	1	SM 2512 sense resistor	0.100 Ω, 1 W, 1%	KOA	SR733ATTER100F
Rcs	1	1/4 W Axial Resistor	510 Ω, 5%	Yageo	CFR−25JB−510R
Rctup1, Rctup2	2	1/4 W Axial Resistor	750 kΩ, 5%	Yageo	CFR−25JB−750K
Rstart1, Rstart2	2	1/4 W Axial Resistor	330 kΩ, 5%	Yageo	CFR−25JB−330K
Rzcd	1	1/4 W Axial Resistor	100 kΩ, 5%	Yageo	CFR−25JB−100k
F1	1	Fuse	2.5 A, 250 V	Littelfuse	37312500430
Connector	2	156 mil 3 pin connector		MOLEX	26−60−4030
Socket	1	8 pin PDIP socket		Mill Max	110−99−308−41−001000
Mechanical	1	Heatsink		Aavid	590302B03600
Mechanical	1	Screw	4−40 1/4 inch screw	Building Fasteners	PMSSS 440 0025 PH
Mechanical	1	Nut	4−40 screw nut	Building Fasteners	HNSS440
Mechanical	1	Nylon Washer	Shoulder washer #4	Keystone	3049
Mechanical	1	TO220 Thermal Pad	9 mil	Wakefield	173−9−240P
Mechanical	4	Standoffs	Hex 4−40, Nylon 0.75”	Keystone	4804k
Mechanical	4	Nylon Nut	Hex 4−40	Building Fasteners	NY HN 440

Appendix 2: Layout Drawings

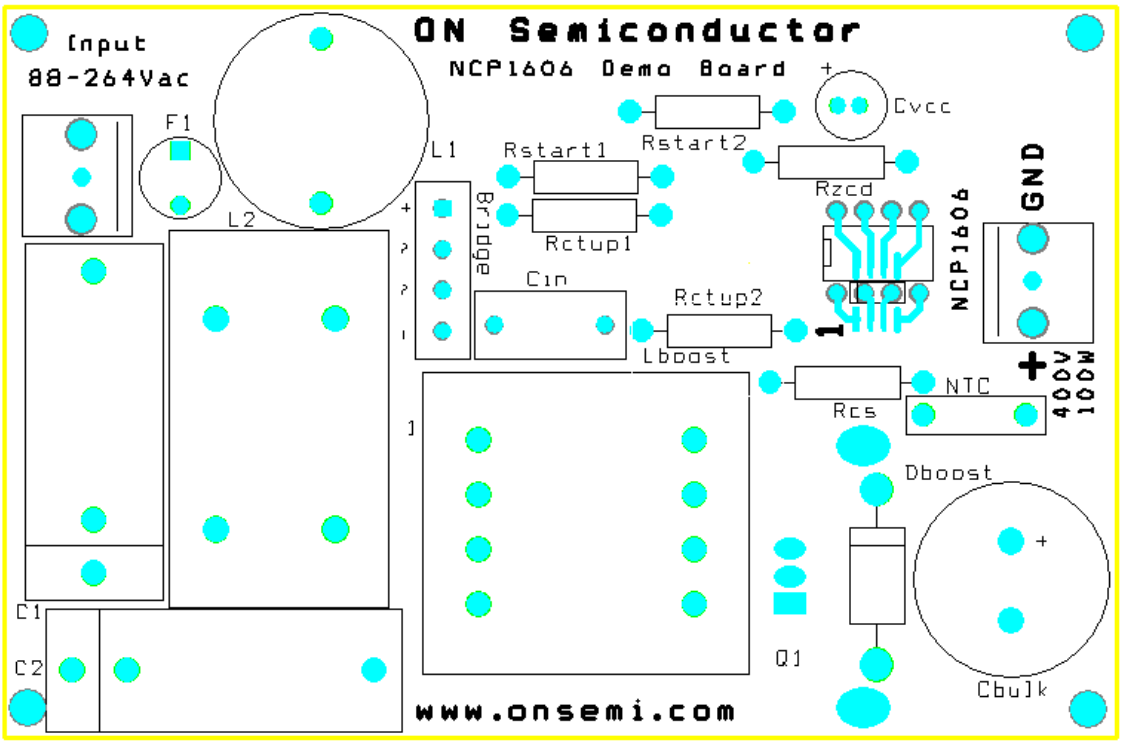

Figure 34. Top View of 100 W Board Layout

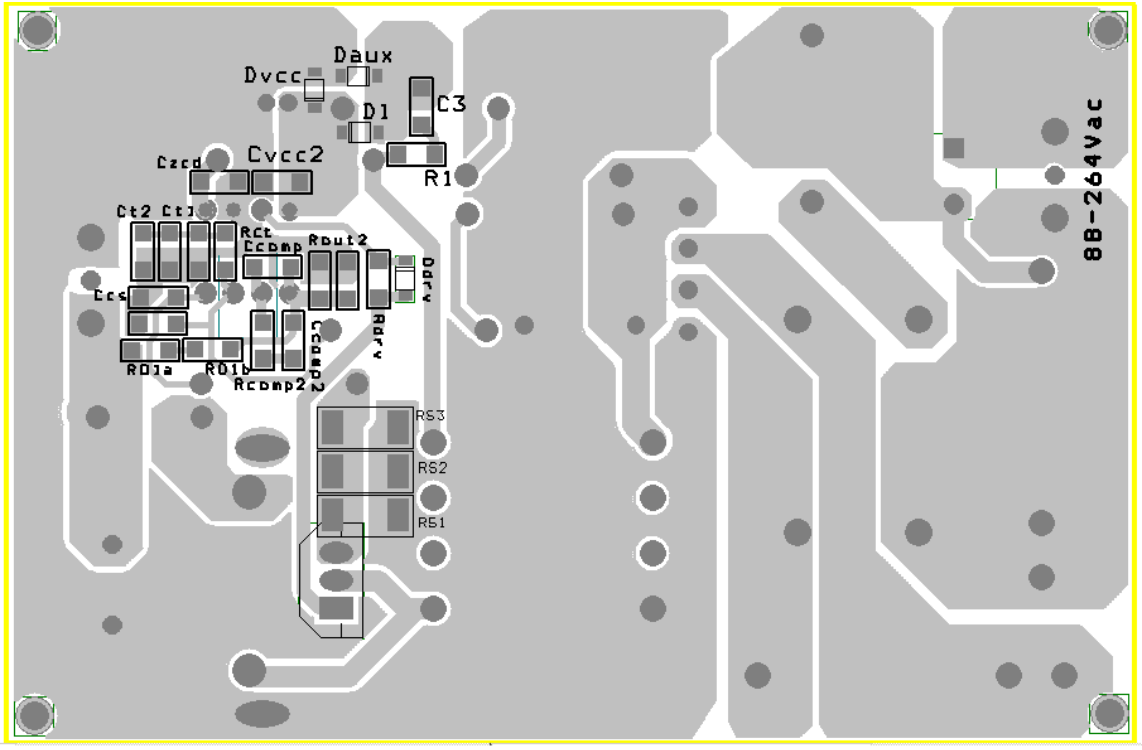

Figure 33. Bottom View of 100 W Board Layout

Appendix 3: Summary of Boost Equations for the NCP1606

RMS Input Current	$I_{ac} = \frac{P_{OUT}}{\eta \cdot V_{ac}}$	η (the efficiency of only the Boost PFC stage) is generally in the range of 90 – 95%
Maximum Inductor Peak Current	$I_{pk(max)} = \frac{2 \cdot \sqrt{2} \cdot P_{OUT}}{\eta \cdot Vac_{LL}}$	Where V_{acLL} is the minimum line input voltage. $I_{pk(max)}$ occurs at the lowest line voltage.
Inductor Value	$L \leq \frac{2 \cdot Vac^2 \cdot \left(\frac{V_{OUT}}{\sqrt{2}} - Vac\right)}{V_{OUT} \cdot Vac \cdot I_{pk(max)} \cdot f_{SW(min)}}$	$f_{SW(min)}$ is the minimum desired switching frequency. The maximum L must be calculated at low line and high line.
Maximum On Time	$t_{on(max)} = \frac{2 \cdot L \cdot P_{OUT}}{\eta \cdot Vac_{LL}^{\ 2}}$	The maximum on time occurs at the lowest line voltage and maximum output power.
Off Time	$t_{off} = \frac{t_{on}}{\frac{V_{OUT}}{Vac \cdot \lvert\sin(\theta)\rvert \cdot \sqrt{2}} - 1}$	The off time is greatest at the peak of the AC line voltage and approaches zero at the AC line zero crossings. Theta (θ) represents the angle of the AC line voltage.
Frequency	$f_{SW} = \frac{Vac^2 \cdot \eta}{2 \cdot L \cdot P_{OUT}} \cdot \left(1 - \frac{Vac \cdot \lvert\sin\theta\rvert \cdot \sqrt{2}}{V_{OUT}}\right)$	
Pin 3 Capacitor	$Ct \geq \frac{2 \cdot P_{OUT} \cdot L \cdot I_{charge}}{\eta \cdot Vac^2 \cdot V_{CTMAX}}$	I_{charge} and V_{CTMAX} are given in the NCP1606 specification table.
Boost Turns to ZCD Turns Ratio	$N_B : N_{ZCD} \leq \frac{V_{OUT} - Vac_{HL} \cdot \sqrt{2}}{V_{ZCDH}}$	Where Vac_{HL} is the maximum line input voltage. The turns ratio must be low enough so as to trigger the ZCD comparators at high line.
Resistor from ZCD winding to the ZCD pin (pin 5)	$R_{ZCD} \geq \frac{Vac_{HL} \cdot \sqrt{2}}{I_{CL(NEG)} \cdot (N_B : N_{ZCD})}$	R_{ZCD} must be large enough so that the shutdown comparator is not inadvertently activated.
Boost Output Voltage	$V_{OUT} = 2.5\ V \cdot \frac{R_{OUT1} + R_{OUT2}}{R_{OUT2}}$	
Maximum V_{OUT} voltage prior to OVP activation and the necessary R_{OUT1} and R_{OUT2}.	$V_{OUT(max)} = V_{OUT(nom)} + R_{OUT1} \cdot I_{OVP}$ $R_{OUT1} = \frac{V_{OUT(max)} - V_{OUT(nom)}}{I_{OVP}}$ $R_{OUT2} = \frac{2.5\ V \cdot R_{OUT1}}{V_{OUT(nom)} - 2.5\ V}$	I_{OVP} is given in the NCP1606 specification table. I_{OVP} is lower for the NCP1606B, then for the NCP1606A version.
Minimum output voltage necessary to exit undervoltage protection (UVP)	$V_{OUT_{(UVP)}} = \frac{R_{OUT1} + R_{OUT2}}{R_{OUT2}} \cdot V_{UVP}$	V_{UVP} is given in the NCP1606 specification table.
Bulk Cap Ripple	$Vripple_{(pk-pk)} = \frac{P_{OUT}}{C_{bulk} \cdot 2 \cdot \pi \cdot f_{line} \cdot V_{OUT}}$	Use f_{line} = 47 Hz for worst case at universal lines. The ripple must not exceed the OVP level for V_{OUT}.
Inductor RMS Current	$Icoil_{(rms)} = \frac{2 \cdot P_{OUT}}{\sqrt{3} \cdot Vac_{LL} \cdot \eta}$	
Boost Diode RMS Current	$Id_{MAX(rms)} = \frac{4}{3} \cdot \sqrt{\frac{2 \cdot \sqrt{2}}{\pi}} \cdot \frac{P_{OUT}}{\eta \cdot \sqrt{Vac_{LL} \cdot V_{OUT}}}$	
MOSFET RMS Current	$I_{M(rms)} = \frac{2}{\sqrt{3}} \cdot \frac{P_{OUT}}{\eta \cdot Vac_{LL}} \cdot \sqrt{1 - \left(\frac{8 \cdot \sqrt{2} \cdot Vac_{LL}}{3\pi \cdot V_{OUT}}\right)}$	

Appendix 3: Summary of Boost Equations for the NCP1606

MOSFET Sense Resistor	$R_{SENSE} = \frac{V_{CS(limit)}}{I_{pk}}$ $P_{RSENSE} = I_{M(rms)}{}^2 \cdot R_{SENSE}$	$V_{CS(limit)}$ is given in the NCP1606 specification table. The NCP1606B has a lower $V_{CS(limit)}$ level.
Bulk Capacitor RMS Current	$I_{C(rms)} = \sqrt{\frac{32 \cdot \sqrt{2} \cdot P_{OUT}{}^2}{9 \cdot \pi \cdot Vac_{LL} \cdot V_{OUT} \cdot \eta^2} - (I_{LOAD(rms)})^2}$	
Type 1 C_{COMP}	$C_{COMP} = \frac{10^{G/20}}{4 \cdot \pi \cdot f_{line} \cdot R_{OUT1}}$	G is the desired attenuation in decibels (dB). Typically it is 60 dB.

The product described herein (NCP1606), may be covered by the following U.S. patents: 5,073,850 and 6,362,067. There may be other patents pending.

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